Low Cost ±300°/sec Yaw Rate Gyro with SPI® Interface

Preliminary Technical Data

ADIS16100

FEATURES

Complete angular rate gyroscope
Z-axis (yaw rate) response
SPI digital output interface
High vibration rejection over wide frequency
2000 *g* powered shock survivability
Externally controlled self-test
Internal temperature sensor output
Absolute rate output for precision applications
5 V single-supply operation
8 mm × 8 mm × 5 mm package

APPLICATIONS

Platform stabilization
Image stabilization
Navigation
Inertial measurement units

GENERAL DESCRIPTION

The ADIS16100 is a complete angular rate sensor (gyroscope) that uses Analog Devices' surface-micromachining process to make a functionally complete and low cost angular rate sensor with an integrated serial port interface, SPI.

The digital data available at the SPI port is proportional to the angular rate about the axis normal to the top surface of the package (see Figure 5). A single external resistor can be used to lower the scale factor. An external capacitor can be used to lower the bandwidth.

Access to an internal temperature sensor measurement is provided, through the SPI port, for compensation techniques. Two pins are available to the user to input analog signals for digitization. An additional output pin provides a precision voltage reference. Two digital self-test inputs electromechanically excite the sensor to test operation of the sensor and the signal conditioning circuits.

The ADIS16100 is available in an 8 mm × 8 mm × 5 mm package.

FUNCTIONAL BLOCK DIAGRAM

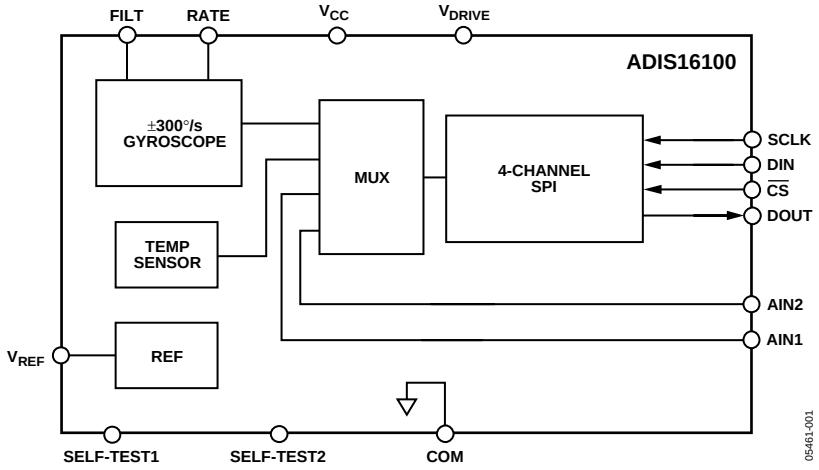

Figure 1.

Rev. PrA

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REVISION HISTORY

3/05—Revision PrA

SPECIFICATIONS

T_A = 25°C, V_{CC} = 5 V, angular rate = 0°/sec , unless otherwise noted.

Table 1.

Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
SENSITIVITY	Clockwise rotation is positive output				
Dynamic Range[2]	Full-scale range over specifications range	±300			°/s
Initial	@25°C	3.75	4.1	4.45	LSB/°/s
Over Temperature[3]	V_{CC} = 4.75 V to 5.25 V	3.75		4.45	LSB/°/s
Nonlinearity	Best fit straight line		0.15		% of FS
Null					
Initial Null		1876	2048	2220	LSB
Over Temperature[3]	V_{CC} = 4.75 V to 5.25 V	1876		2220	LSB
Turn-On Time	Power on to ±½°/s of final		35		ms
Linear Acceleration Effect	Any axis		0.82		LSB/*g*
Voltage Sensitivity	V_{CC} = 4.75 V to 5.25 V		4.1		LSB/V
NOISE PERFORMANCE	0.1 Hz to 1 Hz		0.33		°/s
Rate Noise Density	F = 100 Hz		0.075		°/s/√Hz
FREQUENCY RESPONSE					
3 dB Bandwidth (User-Selectable)[4]	Internal 22 nF as compensation capacitor		40		Hz
Sensor Resonant Frequency			14		kHz
SELF-TEST INPUTS					
ST1 RATEOUT Response[5]	ST1 pin from Logic 0 to Logic 1	−121	−221	−371	LSB
ST2 RATEOUT Response[5]	ST2 pin from Logic 0 to Logic 1	+121	+221	+371	LSB
Logic 1 Input Voltage	Standard high logic level definition	3.3			V
Logic 0 Input Voltage	Standard low logic level definition			1.7	V
Input Impedance	To common		50		kΩ
TEMPERATURE SENSOR					
Reading at 298°K			2048		LSB
Scale Factor	Proportional to absolute temperature		6.88		LSB/°K
2.5 V REFERENCE					
Voltage Value		2.45	2.5	2.55	V
Load Drive to Ground	Source		100		µA
Load Regulation	0 µA < I_{OUT} < 100 µA		5.0		mV/mA
Power Supply Rejection	4.75 V_{CC} to 5.25 V_{CC}		1.0		mV/V
Temperature Drift	Delta from 25°C		5.0		mV
LOGIC INPUTS					
Input High Voltage, V_{INH}		0.7 × V_{DRIVE}			V
Input Low Voltage, V_{INL}				0.3 × V_{DRIVE}	V
Input Current, I_{IN}	Typically 10 nA	−1		1	µA
Input Capacitance, C_{IN}				10	pF
ANALOG INPUTS					
Resolution			12		Bits
Integral Nonlinearity		−2		2	LSB
Differential Nonlinearity		−2		2	LSB
Offset Error		−8		8	LSB
Gain Error		−2		2	LSB
Input Voltage Range		0		VREF × 2	V
Leakage Current		2		2	µA
Input Capacitance			20		pF
Full Power Bandwidth		−8		8	MHz

DIGITAL OUTPUTS					
Output High Voltage (V_{OH})	I_{SOURCE} = 200 µA	V_{Drive} – 0.2			V
Output Low Voltage (V_{OL})	I_{SINK} = 200 µA			0.4	V
Conversion Rate					
Conversion Time	16 SCLK cycles with SCLK at 20 MHz			800	ns
Throughput Rate				1	MSPS
POWER SUPPLY					
V_{CC}		4.75	5	5.25	V
V_{Drive}		2.7		5.25	V
V_{CC} Quiescent Supply Current	V_{CC} @ 5 V, f_{SCLK} = 50 kSPS		7.0	9.0	mA
V_{Drive} Quiescent Supply Current	V_{Drive} @ 5 V, f_{SCLK} = 50 kSPS		1.0		mA
Power Dissipation	V_{CC} and V_{Drive} @ 5 V, f_{SCLK} = 50 kSPS		40		mW

[1] All minimum and maximum specifications are guaranteed. Typical specifications are not tested or guaranteed.
[2] Dynamic range is the maximum full-scale measurement range possible, including output swing range, initial offset, sensitivity, offset drift, and sensitivity drift at 5 V supplies.
[3] Specification refers to the maximum extent of this parameter as a worst-case value of T_{MIN} or T_{MAX}.
[4] Frequency at which the response is 3 dB down from dc response. Bandwidth = 1/(2 x π x 180K x (22 nF + C)). For C = 0, bandwidth = 40 Hz. For C = 1 µF, bandwidth = 0.87 Hz.
[5] Self-test response varies with temperature.

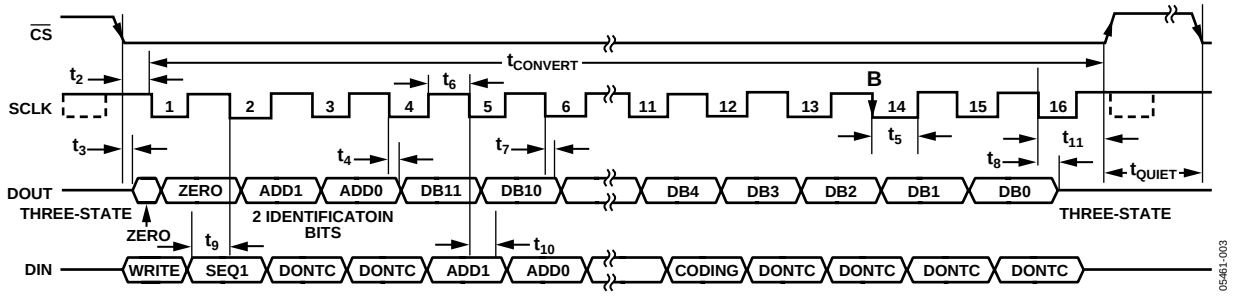

Figure 2. Gyroscope Serial Interface Timing Diagram

TIMING SPECIFICATIONS

T_A = 25°C, angular rate = 0°/sec, unless otherwise noted.

Table 2.

Parameter[1]	V_{DD} = 5	Unit	Description
f_{sclk} [2]	10	kHz min	
	20	MHz max	
$t_{convert}$	16 × t_{sclk}		
t_{quiet}	50	ns min	Minimum QUIET TIME required between $\overline{CS}$ rising edge and start of next conversion.
t_2	10	ns min	$\overline{CS}$ to SCLK setup time.
t_3[3]	30	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled.
t_4[3]	40	ns max	Data access time after SCLK falling edge.
t_5	0.4 x t_{sclk}	ns min	SCLK low pulse width.
t_6	0.4 x t_{sclk}	ns min	SCLK high pulse width.
t_7	10	ns min	SCLK to DOUT valid hold time.
t_8[4]	15/35	ns min/max	SCLK falling edge to DOUT high impedance.
t_9	10	ns min	DIN setup time prior to SCLK falling edge.
t_{10}	5	ns min	DIN hold time after SCLK falling edge.
t_{11}	20	ns min	16th SCLK falling edge to $\overline{CS}$ high.
t_{12}	1	us max	Power-up time from full power-down/auto shutdown modes.

[1] Guaranteed by design. All input signals are specified with t_r and t_f = 5ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit in Figure 3 and defined as the time required for the output to cross 0.4 V or 0.7 V × V_{Drive}.
[4] t_s is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

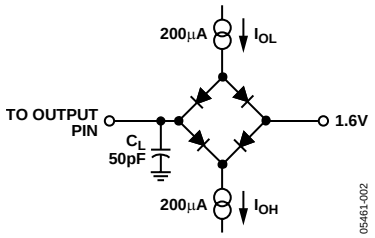

Figure 3. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration (Any Axis, Unpowered, 0.5 ms)	2000 *g*
Acceleration (Any Axis, Powered, 0.5 ms)	2000 *g*
$+V_{CC}$ to COM	–0.3 V to +6.0 V
$+V_{Drive}$ to COM	–0.3 V to V_{CC} + 0.3 V
Analog Input Voltage to COM	–0.3 V to V_{CC} +0.3 V
Digital Input Voltage to COM	–0.3 V to 7.0 V
Digital Output Voltage to COM	–0.3 V to V_{CC} +0.3 V
STx Input Voltage to COM	–0.3 V to V_{CC} +0.3 V
Operating Temperature Range	–40°C to +85°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Drops onto hard surfaces can cause shocks of greater than 2000 *g* and exceed the absolute maximum rating of the device. Care should be exercised in handling to avoid damage.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

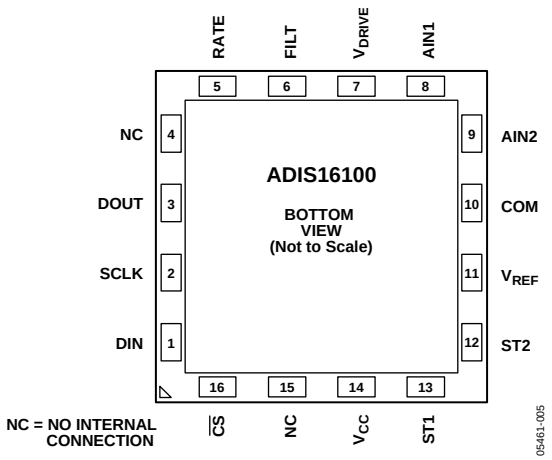

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	DIN	I	Data In. Data to be written to the control registers is provided on this input and is clocked in on the rising edge of the SCLK.
2	SCLK	I	Serial Clock. SCLK provides the serial clock for accessing data from the part and writing serial data to the control registers.
3	DOUT	O	Data Out. The data on this pin represents data being read from the control registers and is clocked on the falling edge of the SCLK.
4	NC		No Connect.
5	RATE	O	External capacitor connection to control bandwidth.
6	FILT	I	External Capacitor connection to control bandwidth.
7	VDRIVE	S	Digital Power.
8	AIN1	I	External Analog Input Channel 1.
9	AIN2	I	External Analog Input Channel 2.
10	COM	S	Common. Reference point for all circuitry in the ADIS16100.
11	V_{REF}	O	Voltage Reference 2.5 V.
12	ST2	I	Self Test Input 2.
13	ST1	I	Self Test Input 1.
14	V_{CC}	S	Analog Power.
15	NC		No Connect.
16	$\overline{CS}$	I	Chip Select. Active low. This input frames the serial data transfer.

THEORY OF OPERATION

RATE SENSITIVE AXIS

This is a z-axis rate-sensing device that is also called a yaw rate sensing device. It produces a positive going output voltage for clockwise rotation about the axis normal to the package top, that is, clockwise when looking down at the package lid.

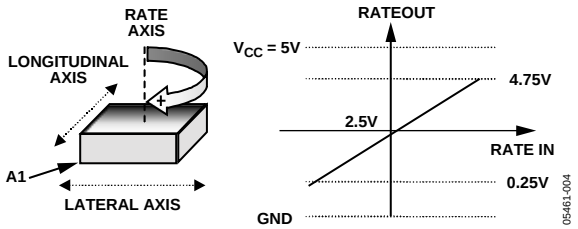

Figure 5. RATEOUT Signal Increases with Clockwise Rotation

OUTLINE DIMENSIONS

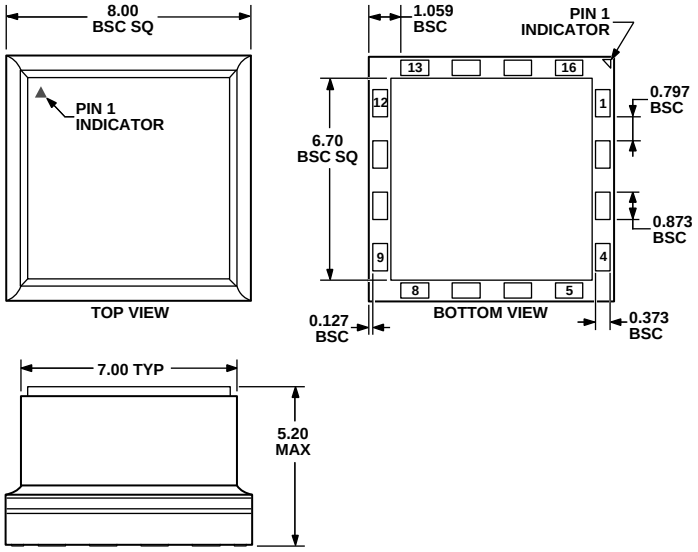

Figure 6. 16-Terminal Land Grid Array [LGA]
(CC-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADIS16100ACC	–40°C to +85°C	16-Terminal Land Grid Array (LGA)	CC-16-2
ADIS16100/PCB	25°C	Evaluation Board	

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